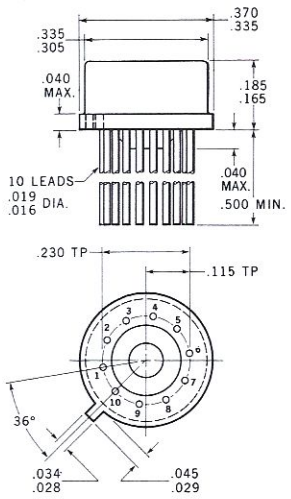
3102
3 INPUT GATE
MOS INTEGRATED CIRCUIT

GENERAL DESCRIPTION — The 3102 is a MOS Monolithic 3-Input Gate Integrated Circuit. This device can be utilized as a vehicle in gaining familiarity with MOS integrated circuit logic versatility, as a building block in an all MOS system, or as a breadboarding gate in designing complex custom integrated circuits. Input protection is provided on all gate inputs.

ABSOLUTE MAXIMUM RATINGS (Note 1)

Storage Temperature	−65°C to +150°C
Operating Temperature	−55°C to +85°C
Positive Voltage on any Pin ($V_{Body} = 0$)	+0.3 Volt
Negative Voltage on any Pin ($V_{Body} = 0$)	−35 Volts
Power Dissipation at $T_A = 25°C$	≤200 mW

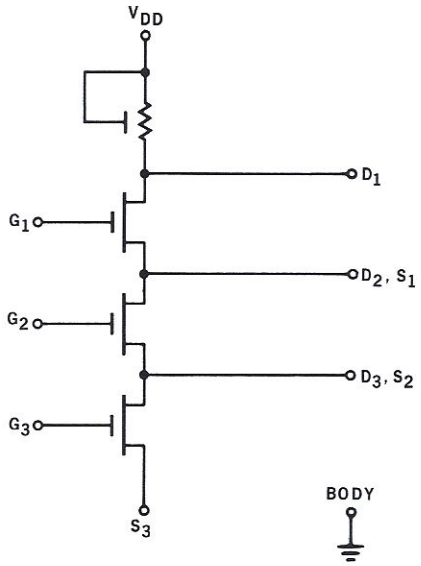
PHYSICAL DIMENSIONS
(In accordance with JEDEC TO-100)



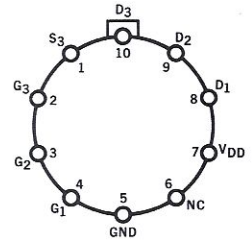
NOTES: All dimensions in inches
Leads are gold-plated Kovar
Package weight is 1.02 grams

ORDER PART NO. A5F3102XXX

SCHEMATIC DIAGRAM



CONNECTION DIAGRAM



TOP VIEW

NOTES:
(1) These ratings are limiting values above which serviceability of the device may be impaired.

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FAIRCHILD SEMICONDUCTOR
A DIVISION OF FAIRCHILD CAMERA AND INSTRUMENT CORPORATION

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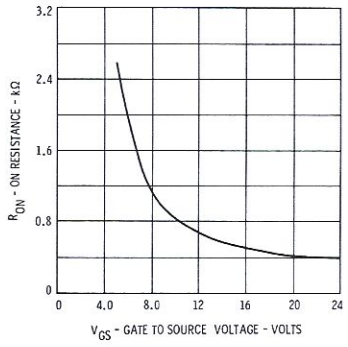
FAIRCHILD MOS INTEGRATED CIRCUIT 3102

ELECTRICAL CHARACTERISTICS ($V_{Body} = 0$; $T_A = 25°C$)

CHARACTERISTICS	CONDITIONS	MIN.	TYP.	MAX.	UNITS
R_{Load}	$V_{DD} = -27\ V \pm 2.0\ V$ $V_{D1} = Gnd$		140		kΩ
R_{ON}(See Figure 1)	$V_{IN} = -20\ V$		500		Ω
Input Leakage Current	$V_{IN} = -25\ V$			1.0	μA
Threshold Voltage (V_{TH})	$V_D = V_G$, $I_D = -10\ \mu A$	−2.0		−5.5	V
Input Capacitance			4.0		pF
Power Consumption	$V_{DD} = -30\ V$, $V_{IN} = -10\ V$		6.0		mW

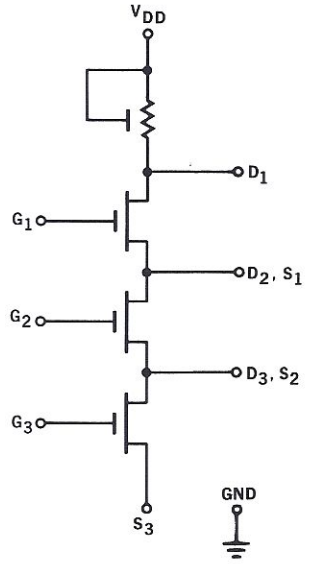
FIG. 1
TYPICAL "ON" RESISTANCE



RESISTANCE CHARACTERISTIC

Parameters	Conditions	TYP.
R_{Load}	$V_{DD} = -25\ V$ $V_{D1} = 0\ V$	140 kΩ
R_{ON}	$V_{GS} = -20\ V$ $V_{DS} \leq -1.0\ V$ $V_{D2} = 0\ V$	500 Ω
R_{ON}	$V_{GS} = -9.0\ V$ $V_{DS} \leq -1.0\ V$ $V_{D2} = 0\ V$	800 Ω

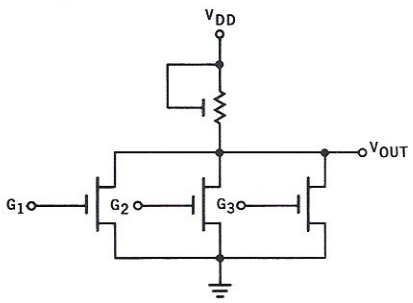
SCHEMATIC DIAGRAM



NOR GATE CONFIGURATION

Pin 8 = Pin 10 = V_{OUT}
Pin 1 = Pin 9 = GND
$V_{DD} = -27\ V \pm 2.0\ V$

	LOGIC LEVEL	VOLTAGE LEVEL MIN.	VOLTAGE LEVEL MAX.
V_{IH}	1	−9.0 V	
V_{IL}	0		−2.0 V
V_{OH}	1	−10 V	
V_{OL}	0		−1.0 V



NAND GATE CONFIGURATION

Pin 5 = GND
Pin 8 = OUTPUT
$V_{DD} = -27\ V \pm 2.0\ V$

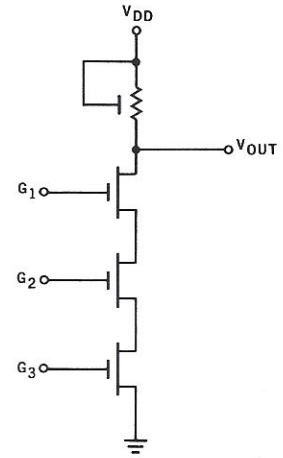


FIG. 2
TYPICAL DRAIN TO SOURCE CHARACTERISTICS

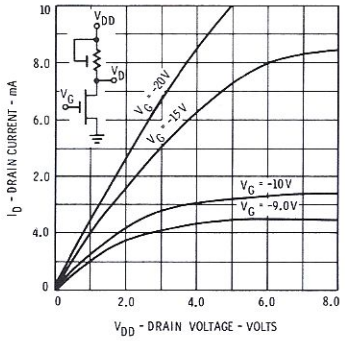
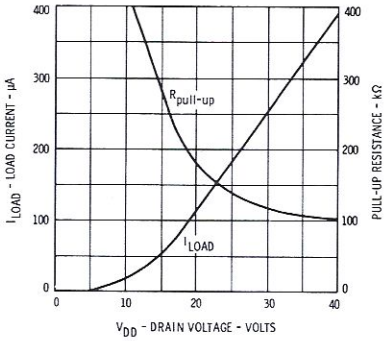
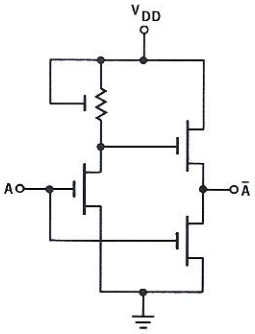


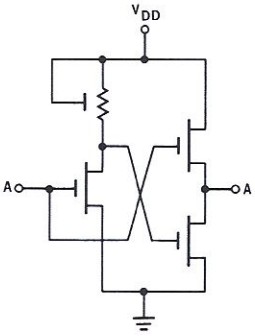
FIG. 3
TYPICAL PULL-UP RESISTANCE



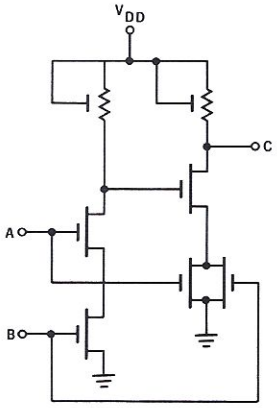
APPLICATIONS — MOS logic will provide the versatility to build many different functions. The following circuits show how to build the functions using one or two 3102 packages.



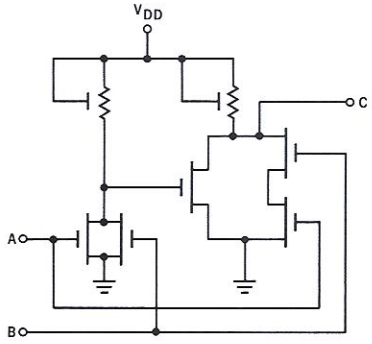
INVERTING BUFFER



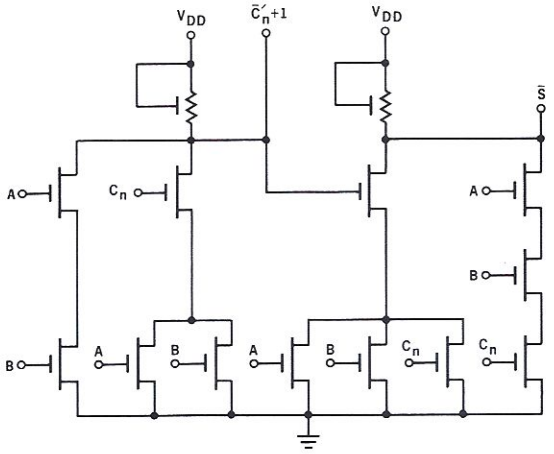
NON-INVERTING BUFFER



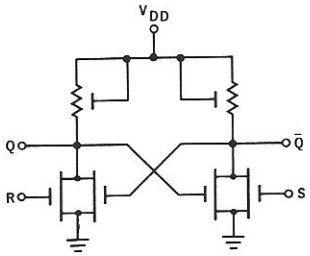
$C = AB + \bar{A}\bar{B}$
EXCLUSIVE NOR



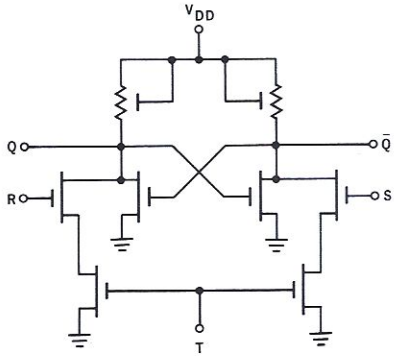
$C = \bar{A}B + \bar{B}A$
EXCLUSIVE OR



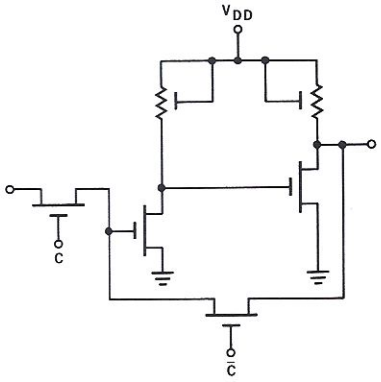
$C'_{n+1} = AB + C_n(A + B)$
$S = (A+B+C_n)\, C'_{n+1} + ABC_n$
FULL ADDER



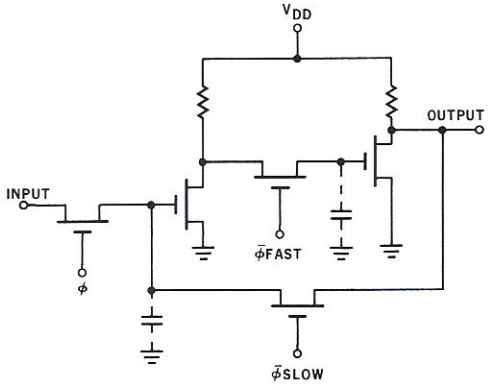
RS FLIP-FLOP



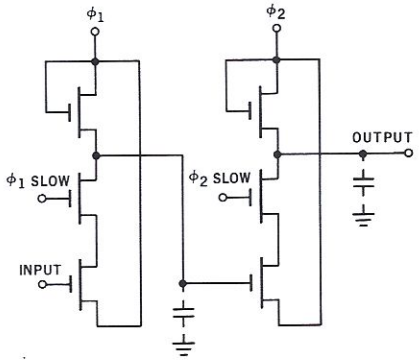
RST FLIP-FLOP



TYPE D FLIP-FLOP



STATIC (DC) SHIFT REGISTER BIT



DYNAMIC 4-PHASE (4ϕ) SHIFT REGISTER BIT

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